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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,656	02/13/2002	Detlev Richter	P2001,0097	9370

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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,656	RICHTER, DETLEV	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 remain in the application. Claims 1, 2 and 11 have been amended. Claims 1-13 have been examined. New drawings for Figures 1-3 have been entered and are accepted by the Examiner.

Drawings

2. The Applicants have overcome the objections to the drawings, according to the Office Action dated 08/02/2004, ¶ 2. The Examiner withdraws the objection and accepts the drawings.

3. The Examiner agrees with the Appicants argument that flowcharts should not be required, as requested in the Office Action dated 08/02/2004, ¶ 3, therefore, the Examiner withdraws the objection.

Specification

4. The Applicants have overcome the objections to the specification, according to the Office Action dated 08/02/2004, ¶ 4. The Examiner withdraws the objection.

Claim Objections

5. The Applicants have overcome the objections to claim 1because of informalities, according to the Office Action dated 08/02/2004, ¶ 5. The Examiner withdraws the objection.

Claim Rejections - 35 USC § 112

6. The rejection of claim 1 under 35 U.S.C. 112, first paragraph, according to the Office Action dated 08/02/2004, ¶ 6, has been overcome by the Applicants. The Examiner withdraws the rejections.

7. The rejection of claims 1-3 under 35 U.S.C. 112, second paragraph, according to the Office Action dated 08/02/2004, ¶ 7, has been overcome by the Applicants. The Examiner withdraws the rejections.

Response to Arguments

8. Applicant's arguments on pages 13 and 14, filed November 2, 2004, with respect to the filing date of the prior art, namely Sanghani (US-2003/0101376) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Bates et al. (US-6477674).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claim 1-5, 7-10, 12 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Bates et al. (US-6477674), hereinafter Bates.

Claims 1, 3-5, 7 and 9:

Bates teaches an integrated circuit (IC) 500 which includes input/output (I/O) buffers 100(1)-100(n) in a block diagram shown in FIG. 5 (**bidirectionally operating interface circuits**). Bates also teaches I/O buffers 100(1)-100(n) make up a data block of I/O circuitry for transmitting to and receiving data from other IC 100 devices (**first and second equally sized groups of interface circuits**). (Col. 4, ll. 28-32). Bates further teaches test pattern generator 210 is coupled to MUX 205 and MUX 115, and is used to generate test pattern signals for testing I/O test circuit 100 upon the initiation of a loopback test (**a first circuit...serving to generate test signals...**). Bates discloses test pattern generator 210 may be implemented with two or more flip flops, **a linear feedback register** (also as per claim 4), **a random pattern generator** (also as per claims 3 and 9) or random access memory (RAM). Bates suggests the test pattern signals may be loaded into test pattern generator 210 from an integrated circuit tester

(not shown) via a test chain prior to conducting a loopback test (**a respective electrical connection... outside of the semiconductor module for enabling a self-test**). Bates teaches compare unit 220 compares test signals received from stage unit 215 with test signals received from amp 145, after having passed through the components of I/O buffer 100 (**a second circuit... for receiving and process test signals...**). Bates also teaches if compare unit 220 detects a difference between the signals received from amp 145 and those received from test pattern generator 210, an error signal is transmitted from compare unit 220 (**a second circuit... for receiving and process test signals...**, also **calculating a signature... and comparing ... with a prescribed signature** as per claims 5 and 9). Bates also teaches the compare unit 220 may be implemented using an Exclusive-Or-Gate or other comparison logic may be used to implement compare unit 220. (Col. 3, l. 46 through col. 4, l. 13). Bates further teaches V_{REF} pad 140 receives an external reference voltage (**a respective separate voltage supply...**). (Col. 2, l. 65).

Claim 2:

"a third circuit connected to said and serving to generate test signals interface circuits of be multiplexed in and output via said second group"

Bates teaches MUX 225 is coupled to compare unit 220 and latch 230. MUX 225 selects signals from compare unit 220 whenever a loopback test is in progress at I/O buffer 110, and selects the scan chain path after the test pattern is complete.

"wherein said second circuit connected to said first group for receiving and processing test signals received via said interface circuits of said first group"

Bates teaches compare unit 220 compares test signals received from stage unit 215 with test signals received from amp 145, after having passed through the components of I/O buffer 100. Bates also teaches if compare unit 220 detects a difference between the signals received from amp 145 and those received from test pattern generator 210, an error signal is transmitted from compare unit 220. (Col. 3, l. 66 through col. 4, l. 13).

Claim 8:

"after processing the test signals output by the first group and received by the second group of interface circuits, reversing a test direction...".

Bates teaches I/O buffers 100(1) and 100(n) support AC I/O loopback testing. Bates also teaches although I/O buffer 100 may be determined to be functional after a standard I/O loopback test, an AC loopback test provides the capability of detecting more subtle defects in the components of I/O buffer 100 that may effect timing. Thus, conducting an AC I/O loopback test examines the AC I/O loopback of the input and output paths of I/O buffer 100(x) (reversing a test direction).

Claim 10:

"influencing a connection of the assigned interface circuits in order to include an influence of interference quantities in the self-test".

Bates suggests the test pattern signals may be loaded into test pattern generator 210 from an integrated circuit tester (not shown) via a test chain prior to conducting a loopback test.

Claim 12 and 13:

"modulating low-frequency signal voltages onto at least one of the supply voltages of the interface groups" as per claim 12.

"modulating two low-frequency sinusoidal signals of different frequency onto both supply voltages" as per claim 13.

Bates teaches V_{REF} pad 140 receives an external reference voltage, differential amplifier (amp) 145 is coupled to I/O pad 135 and V_{REF} pad 140 and amp 145 aggregates signals received from I/O pad 135 and V_{REF} pad 140 into a single signal. Bates also teaches amp 145 transmits a logical one whenever a signal received at I/O pad 135 is higher in magnitude than a signal received at V_{REF} pad 140. Bates further teaches amp 145 transmits a logical zero whenever a signal received at I/O pad 135 is lower in magnitude than a signal received at V_{REF} pad 140. However, it is understood by one of ordinary skill in the art that the operation of amp 145 may be reversed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bates et al. (US-6477674), hereinafter Bates, in view of Takagi (US-6704897), hereinafter Takagi.

Claim 6:

Bates does not explicitly teach a multiple input shift register (MISR) fro receiving and processing test signals. However, Bates does teach compare unit 220 may be implemented using an Exclusive-Or-Gate or other comparison logic. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bates' compare unit 220 with Takagi compaction circuit 13 (MISR). The artisan would have been motivated to do so because this would enable Bates' compare unit 220 to further evaluate consecutively store the resulting random data Takagi's flip flop 70'.

11. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bates et al. (US-6477674), hereinafter Bates, in view of Levy et al. (US-5751151), hereinafter Levy.

Claim 11:

Bates does not explicitly teach of the influencing step consisting of resistive, capacitive and inductive. However, Levy suggests when VDD potential is to be applied to the corresponding pin of the DUT 10A and 10B, a corresponding relay coil, such as the relay coil 30 (inductive influence), is operated to pull the contact 26 from its lower position to its upper position, where it then is attached to a source or operating potential (VDD) as illustrated in FIG. 1. (Col. 4, lines 28-33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bates' testing method to include Levy's method of applying VDD influences via the corresponding relay coils. The artisan would have been motivated to do so because this would give Bates more flexibility in applying power sources to the DDR I/O interface circuits during testing.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

Guy J. Lamarre
Primary Examiner